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| 23413               | 7590        | 11/03/2009           | EXAMINER            |                  |
| CANTOR COLBURN, LLP |             |                      | BODDIE, WILLIAM     |                  |
| 20 Church Street    |             |                      |                     |                  |
| 22nd Floor          |             |                      | ART UNIT            | PAPER NUMBER     |
| Hartford, CT 06103  |             |                      | 2629                |                  |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

[usptopatentmail@cantorcolburn.com](mailto:usptopatentmail@cantorcolburn.com)

|                              |                        |                     |  |
|------------------------------|------------------------|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |  |
|                              | 10/756,939             | PARK, JIN-HO        |  |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |  |
|                              | WILLIAM L. BODDIE      | 2629                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 03 September 2009.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-11 and 14-17 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-11 and 14-17 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

|                                                                                      |                                                                   |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .                                                        | 6) <input type="checkbox"/> Other: _____ .                        |

## DETAILED ACTION

1. In an amendment dated, September 3<sup>rd</sup>, 2009, the Applicant amended claims 1 and 7. Currently claims 1-11, 14-17 are pending.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-11, 14-17 have been fully considered but are not persuasive.
3. On pages 7-8 of the Remarks, the Applicant concede that Kawaguchi teaches "broadly and generally that an *undefined delay* of a signal line is "inherent" due to the material." Applicant argues that Kawaguchi does not provide, inherently or otherwise, that the image signal is delayed substantially the same amount as a gate driving signal.
4. The Examiner broadly and generally agrees with Applicant's description of the teachings of Kawaguchi. Kawaguchi is seen to provide a resistive load on the output instruction signal line, which in turn imparts an inherent yet undefined amount of delay. Furthermore the delay of the gate lines, which is substantially caused by **both** resistive and capacitive loads, is not equivalent to the amount of delay of the output instruction signal line of Kawaguchi.

In other words, Kawaguchi's disclosure results in an inherent output instruction signal delay due solely to the resistive properties of the signal line itself. However, this delay, caused by the resistive properties alone, is not equivalent to the delay of the gate signal. The delay of the gate signal of Kawaguchi is caused by not only a similar resistive load as the output instruction signal line, but also a capacitive load which is caused by the arrangement of the common electrode and the gate line.

On pages 9-10 of the Remarks, the Applicant argues that Nakamura does not disclose any timing effect of locating wiring signals opposing a common electrode.

5. While Examiner agrees that Nakamura does not expressly disclose a timing effect, there will nonetheless be a delay caused by both the resistive and capacitive loads formed by the metallic material of the signal line electrode and the arrangement of the electrodes, respectively. As has been discussed in previous office actions, Applicant discloses that simply by the virtue of the material properties and arrangement of electrodes a specific delay is created in a signal line (page 3, lines 2-5). It is the arrangement of the signal lines of Nakamura in relation to the common electrode that is incorporated into the display of Kawaguchi. Locating the output instruction signal line of Kawaguchi under the common electrode as taught by Nakamura results in a structurally similar display to that of the Applicant.

6. As such the rejections of the claims have been updated to address the current amendments but have otherwise been maintained.

#### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-5, 7-9, 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Nakamura et al. (US 7,136,058).

**With respect to claim 1,** Kawaguchi discloses, an LCD apparatus comprising:  
an LCD panel (221 in fig. 30) displaying images (col. 15, lines 27-42) and  
including:

a first substrate (228 in fig. 30);  
a second substrate facing the first substrate (227 in fig. 30), a plurality of pixels  
being provided on the second substrate (fig. 1; col. 18, lines 39-45);  
gate lines (x-axis in fig. 30, for example) disposed on the second substrate and  
opposing the first substrate (fig. 30), the gate lines receiving a gate driving signal;  
data lines for supplying image data signals to the pixels (3 in fig. 1, for example;  
col. 31, lines 13-16); and  
an output instruction signal line (231 in figs. 30-32) disposed on the second  
substrate (figs. 1, 33) transmitting an output instruction signal;  
a data driver (6 y-axis ICs; 229 in fig. 30) disposed on a data tape carrier  
package (TCP) (230 in figs. 30-32);  
a gate driver (4 x-axis ICs in fig. 30) outputting a gate driving signal to the LCD  
panel; and  
a timing controller (8 in fig. 1; col. 19, lines 15-18; 232 in fig. 30; col. 28, lines 6-  
14) providing a first control signal (x-axis 231 in fig. 30) to the gate driver so as to  
control an output of the gate driving signal and providing the output instruction signal (y-  
axis 231 in fig. 30) to the data driver via the output instruction signal line (col. 25, lines  
3-12) to delay the output instruction signal depending on a resistive load formed by the

output instruction signal line (the output instruction signal line will inherently consist of a resistive load that will delay the output instruction signal),

wherein the output instruction signal line is disposed between the data TCP and the gate lines (gate lines are seen as the parallel lines that are output from 4 x-axis ICs, in fig. 30, into the panel, while the data TCP is seen as 230 in fig. 30; should be clear from fig. 30 that the output instruction signal line is disposed between the TCP and the gate lines), and

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instructions signal is delayed (the resistive load attributed to the metallic signal line which provides the output instruction signal will inherently cause delay, each data driver in fig. 30 will thus be at least slightly delayed in outputting the data signal).

Kawaguchi does not expressly disclose a common electrode disposed on the first substrate; or that the output instruction signal line opposes the common electrode.

Nakamura discloses, an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);

a common electrode disposed on the first substrate (col. 4, lines 17-19);  
gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and

signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to

being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal lines of Kawaguchi so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

Upon combining, as discussed above in the Response to Arguments section, the delay time of the image signal will be substantially equal to a delayed time of the gate driving signal. For further discussion see above discussion in response to Applicant's remarks.

**With respect to claim 2,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 1 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 30).

**With respect to claim 3,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 2 (see above).

Kawaguchi further discloses, comprising a plurality of signal transmission members (246, 248 in fig. 32; for example) electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives the output instruction signal from timing controller via one of the signal transmission members (note the connection of 231 with 242 and 240 in fig. 32).

**With respect to claim 4,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 3 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises:  
the gate lines (note the outputting gate lines from the y-axis ICs in fig. 30) receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a second direction substantially perpendicular to the first direction (fig. 30); and

a plurality of data lines (x-axis ICs in fig. 30) receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

**With respect to claim 5,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is extended in the first direction and is substantially parallel to the gate lines (seems clear from figs. 30-32).

**With respect to claim 7,** Kawaguchi discloses, an LCD apparatus comprising:  
an LCD panel (221 in fig. 30) displaying images (col. 15, lines 27-42) and including:

a first substrate (228 in fig. 30);  
a second substrate facing the first substrate (227 in fig. 30), a plurality of pixels being provided on the second substrate (fig. 1; col. 18, lines 39-45);  
gate lines (x-axis in fig. 30, for example) disposed on the second substrate and opposing the first substrate (fig. 30), the gate lines receiving a gate driving signal;  
data lines for supplying image data signals to the pixels (3 in fig. 1, for example; col. 31, lines 13-16); and  
an output instruction signal line (231 in figs. 30-32) disposed on the second substrate (figs. 1, 33) transmitting an output instruction signal;  
a data driver (6 y-axis ICs; 229 in fig. 30) disposed on a data tape carrier package (TCP) (230 in figs. 30-32);  
a gate driver (4 x-axis ICs in fig. 30) outputting a gate driving signal to the LCD panel; and  
a timing controller (8 in fig. 1; col. 19, lines 15-18; 232 in fig. 30; col. 28, lines 6-14) providing a first control signal (x-axis 231 in fig. 30) to the gate driver so as to control an output timing of the gate driving signal and providing the output instruction signal (y-axis 231 in fig. 30) to the data driver data via the output instruction signal line (col. 25, lines 3-12) to delay the output instruction signal depending on a resistive load formed by the output instruction signal line (the output instruction signal line will inherently consist of a resistive load that will delay the output instruction signal); and  
a plurality of signal transmission members (246, 248 in fig. 32; for example) electrically connecting the data driver with the LCD panel;

wherein the output instruction signal line provides the output instruction signal to the data driver via one of the signal transmission members (note the connection of 231 with 242 and 240 in fig. 32); and

wherein the output instruction signal line is disposed between the data TCP and the gate lines (gate lines are seen as the parallel lines that are output from 4 x-axis ICs, in fig. 30, into the panel, while the data TCP is seen as 230 in fig. 30; should be clear from fig. 30 that the output instruction signal line is disposed between the TCP and the gate lines); and

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instructions signal is delayed (the resistive load attributed to the metallic signal line which provides the output instruction signal will inherently cause delay, each data driver in fig. 30 will thus be at least slightly delayed in outputting the data signal).

Kawaguchi does not expressly disclose a common electrode disposed on the first substrate; or that the output instruction signal line opposes the common electrode.

Nakamura discloses an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);  
a common electrode disposed on the first substrate (col. 4, lines 17-19);  
gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and  
signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a

capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal lines of Kawaguchi so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

Upon combining, as discussed above in the Response to Arguments section, the delay time of the image signal will be substantially equal to a delayed time of the gate driving signal. For further discussion see above discussion in response to Applicant's remarks.

**With respect to claim 8,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 7 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises: the gate lines (note the outputting gate lines from the ICs in fig. 30) extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines (x-axis lines in fig. 30) extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and

design of a matrix panel using the gate and data lines oriented in the way currently claimed).

**With respect to claim 9,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 8 (see above).

Kawaguchi further discloses, wherein the output instruction line is extended in the first direction (clear from fig. 30).

**With respect to claim 11,** Kawaguchi, and Nakamura disclose, the LCD apparatus of claim 7 (see above).

Kawaguchi further discloses, wherein the signal line is formed on the LCD panel and adjacent to the data driver (clear from fig. 30).

**With respect to claim 14,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 1 (see above).

Kawaguchi, when combined with Kubota and Nakamura, further discloses, comprising a plurality of signal transmission members (Kawaguchi; 246, 248 in fig. 32; for example) electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives the output instruction signal from timing controller via one of the signal transmission members (Kawaguchi; note the connection of 231 with 242 and 240 in fig. 32).

**With respect to claim 15,** Kawaguchi and Nakamura disclose the LCD apparatus of claim 1 (see above).

Kawaguchi, when combined with Nakamura, further discloses wherein capacitive and resistive loads of the gate lines and the output instruction signal line are

substantially equal to each other (Kawaguchi discloses that the output instruction line and the gate lines are formed on the same substrate. This is seen as sufficient to generate capacitive and resistive loads that are substantially equal to one another. As discussed by the Applicants on page 13, lines 16-23, all that is attributed to the two lines having equal loads is that they are formed on the same substrate).

**With respect to claim 16,** Kawaguchi and Nakamura disclose the LCD apparatus of claim 1 (see above).

Kawaguchi, when combined with Nakamura, further discloses wherein a delay of providing the output instruction signal to the data driver is substantially equal to the delay of the gate driving signal (Kawaguchi discloses that the output instruction line and the gate lines are formed on the same substrate. This is seen as sufficient to delay the two signals an equal amount. As discussed by the Applicants on page 13, lines 16-23, all that is attributed to the two lines having equal delays is that they are formed on the same substrate).

**With respect to claim 17,** Kawaguchi and Nakamura disclose the LCD apparatus of claim 1 (see above).

Kawaguchi further discloses, wherein a portion of the output signal line is disposed on the data driver (fig. 30's mapping of the output signal line is very similar to that shown in Applicant's own figure 4; also note fig. 32 of Kawaguchi which shows the output signal line connecting and extending onto the flexible circuit board (236,242,255) and eventually the data driver).

9. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Nakamura et al. (US 7,136,058) and further in view of Kubota et al. (US 6,791,526).

**With respect to claim 6,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area (col. 1, lines 62-67).

Kubota, Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor namely control circuitry design for LCD panels.

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

**With respect to claim 10,** Kawaguchi and Nakamura disclose, the LCD apparatus of claim 9 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal and the image data are substantially simultaneously provided to a corresponding pixel area (col. 1, lines 62-67).

Kubota, Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor namely control circuitry design for LCD panels.

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

### ***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William L Boddie/  
Examiner, Art Unit 2629  
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